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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,147	03/19/2004	N. Johan Knall	MA-002-1-I-b	8647

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MATRIX SEMICONDUCTOR
3230 Scott Blvd
Santa Clara, CA 95054

EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,147	KNALL ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a stacked memory structure having a conductive rail that may be silicide, an antifuse that may include silicon dioxide, and a diode structure, does not reasonably provide enablement for a generically usable or broad semiconductor structure specifically having the claimed layer structure. The specification is completely silent as to the form, utility, or purpose of any generic semiconductor structures having the claimed layering that are not part of a memory cell of a stacked structure.

The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

2. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The invention as claimed appears to read on the embodiment of figure 5, since all other disclosed embodiments have the antifuse layer surrounded by doped semiconductor material and not abutting the conductive rail layer. Although earlier in the specification, a vast number of materials are disclosed as viable for both the conductor and the antifuse layer, there is no

suggestion anywhere in the specification that it would be viable or appropriate to use a silicide conductor in a configuration directly abutting a silicon oxide antifuse. Hence, it is unclear from the specification that the specific combination of silicide (or cobalt silicide in claim 2) as the conductor layer (105 or 113) and silicon oxide as the antifuse (106 or 112) would be specifically appropriate or advantageous in the embodiment of figure 5.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,300,664 to Kuroi et al.

Kuroi discloses a semiconductor structure (figure 20) comprising: a first silicide layer (8); a silicon dioxide layer (36) on and in contact with the first silicide layer (gate oxide extends over silicide layer); a 'first' lightly doped semiconductor layer on and in contact with the silicon dioxide (portion of gate electrode nearest the gate oxide interface at 2000 angstroms depth – see figures 8, 12, 21); and a 'second' heavily doped semiconductor layer (upper or peak dopant portion of gate electrode portion in figures 8, 12, 21) on and in contact with the lightly doped

region. It is noted that since the claim is a device claim, rather than a method claim, and since the only feature delineating the first and second semiconductor layers is the dopant concentration, a 'single layer' structure having a graded profile is substantially identical to a two layer structure with different dopant concentration, particularly when dopant migration is taken into account.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. in view of U.S. Patent No. 4,378,628 to Levinstein et al.

Kuroi fails to specifically disclose that the silicide is cobalt silicide.

Levinstein teaches that for MOSFET structures, the silicide contact layer on the source and drain is cobalt silicide (column 1, lines 10-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically choose CoSi, as suggested by Levinstein, in the device of Kuroi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use CoSi, because Levinstein shows that usage of cobalt silicide as the source and drain contact is notoriously old and well-known in the art (Levinstein, column 1, lines 10-20), and CoSi provides the well known advantages of suitable selective etching properties (Levinstein, column

2, lines 40-45), compatibility with subsequent semiconductor and metal depositions (Levinstein, column 2,lines 55-62), as well as low contact resistance (Levinstein, column 2, line 63-column 3, line 5).

7. Claims 1 and 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,034,882 to Johnson et al. in view of U.S. Patent No. 5,451,811 to Whitten et al.

Regarding the claims, Johnson discloses a semiconductor structure comprising: a first silicide layer (all rail layers 20, 21, 46, 48, 50; see column 13, lines 45-50; column 14, lines 42-65 – silicide is listed as an appropriate material for the metal rail conductors); an antifuse stacked thereon (23; layers 42 and 43 are antifuse layers–column 12, lines 5-8; also see column 5, lines 55-65 and column 7, lines 47-57, noting that for discrete devices, changing the orientation of the device (i.e., turning the device upside down), does not alter the device); and a stacked diode with a lightly doped layer adjacent to the antifuse and a heavily doped layer thereon ('steering' element 22, formed by diode 40+41; column 7, lines 57-67; column 12, lines 1-12; also see figure 6(a), upper left portion). Regarding claims 3-6, Johnson discloses that the antifuse is a rupture-type antifuse comprising silicon oxide that is breached, forming a diode or Schottky diode (column 6, lines 8-15; column 7, line 60 – column 8, line 5; column 8, lines 45-67; column 12, lines 1-20). Regarding claims 7, 8, and 9, Johnson discloses that the structure is a portion of a memory level, and may have other layers disposed above or below (see figures 5, 6g, 7).

Johnson, however, teaches that the antifuse is a stack of a silicon oxide and a silicon layer, rather than being a single layer of silicon oxide.

Whitten teaches that silicon dioxide layers, silicon layers, or any combination of the two are equivalently and interchangeably usable as antifuse layers directly contacting an electrode layer (see column 4, lines 40-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory structure of Johnson, such that silicon oxide alone, rather than a silicon oxide/silicon stack, is used as the antifuse, as suggested by Whitten. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a single silicon oxide layer, because Whitten shows that single silicon oxide layers are suitable for use as an antifuse layer in a programmable memory structure. Since Whitten shows that silicon oxide layers and combinations of silicon oxide and silicon can be interchangeably used as rupture antifuses (see Whitten, column 4, lines 40-50, and hence comprise alternate materials known to be suitable for the same purpose, it is well within the purview of a person skilled in the art to select from any of these known materials when forming an antifuse layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER